

AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

Sub B1 1. (Currently Amended) A microcomputer including a read-only memory that stores programs, a controller/calculator that successively accesses ~~[[to]]~~ addresses of the programs stored in said read-only memory to retrieve and decode an instruction from each of the accessed addresses, ~~thereby executing~~ to execute a processing process based on the decoded instruction, and a program counter in which an address to be accessed by ~~said the~~ controller/calculator is successively renewed ~~and indicated~~, said microcomputer comprising

at least one comparison-address-storage device that stores a comparison address data corresponding to an optional address of the programs stored in ~~said the~~ read-only memory, at which ~~an interruption-processing should be~~ interruption-process is executed to virtually revise the programs stored in ~~said the~~ read-only memory;

a random-access memory that stores a revisional program in which ~~said interruption-processing the interruption-process~~ is programmed;

at least one vector-address-storage device that stores a vector address data corresponding to a head address of ~~said revision the revisional~~ program stored in said random-access memory; and

an address comparator that compares ~~said the~~ comparison address data with an address successively renewed in ~~said the~~ program counter;

wherein ~~said the~~ controller/calculator ~~makes an access to~~ accesses the head address of ~~said the~~ revisional program, stored in said random-access memory, corresponding to ~~said the~~ vector

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address data stored in said vector-address-storage device, when it there is a coincidence between said the comparison address data and the renewed address of said the program counter, resulting in an execution of ~~said interruption-processing~~ the interruption-process in accordance with ~~said the~~ revisional program;

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a return-address-setter that sets return-address data in the program counter to coincide with the comparison address data when execution of the interruption-process in accordance with the revisional program is completed; and

an address-coincidence-disabling system that disables the coincidence between the comparison address data and the return-address set in the program counter by said return-address-setter.

2. (Currently Amended) A microcomputer as set forth in claim 1, further comprising:

a discrimination system that discriminates whether the coincidence between ~~said the~~ comparison address data and the renewed address of said program counter is proper; and

an address-coincidence-disabling system that disables the coincidence between ~~said the~~ comparison address data and the renewed address of ~~said the~~ program counter.

3. (Currently Amended) A microcomputer as set forth in claim 1, further comprising:

a rewritable and non-volatile memory that stores said revisional program, ~~said the~~ comparison address data and said vector address data; and

a reading/writing system that reads ~~said the~~ revisional program, ~~said the~~ comparison address data and ~~said the~~ vector address data from said rewritable and non-volatile memory, and ~~then~~ writes ~~these data~~ the revisional program, the comparison address data and the vector address data in said

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random-access memory, said comparison-address-storage device and said vector-address-storage device, respectively, whenever the microcomputer is powered ON.

4. (Currently Amended) A microcomputer as set forth in claim 1, wherein said address comparator is connected to ~~said the~~ program counter to ~~thereby~~ retrieve the renewed address ~~therefrom~~.

5. (Currently Amended) A microcomputer as set forth in claim 1, wherein said address comparator is connected to an address bus extending to ~~said the~~ program counter, to ~~thereby~~ retrieve the renewed address ~~therefrom~~ from the program counter.

6. (Currently Amended) A microcomputer as set forth in claim 1, further comprising a vector-address data setting system that reads the vector address data from said vector-address-storage device, and sets the vector-address-data ~~is then set in said the~~ program counter, ~~whereby the enabling~~ access to the head address of ~~said the~~ revisional program by said controller/calculator ~~is made,~~ ~~resulting in the~~ and execution of ~~said interruption-processing~~ the interruption-process in accordance with ~~said the~~ revisional program.

7. (Currently Amended) A microcomputer as set forth in claim 1, further comprising:
a vector-address-temporary-storage device that receives the vector address data from said vector-address-storage device, when it is ~~determined by~~ said address comparator determines that there is ~~the~~ coincidence between ~~said the~~ comparison address data and the renewed address of ~~said the~~ program counter; and

a vector-address data setting system that reads the vector address data from said vector-address-temporary-storage device, and ~~is then set in said~~ sets the vector-address-data in the program

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2 counter, ~~whereby enabling~~ the access to the head address of ~~said the~~ revisional program by said controller/calculator is made, ~~resulting in the~~ and execution of ~~said interruption-processing the~~ interruption process in accordance with ~~said the~~ revisional program.

Claim 8. canceled.
